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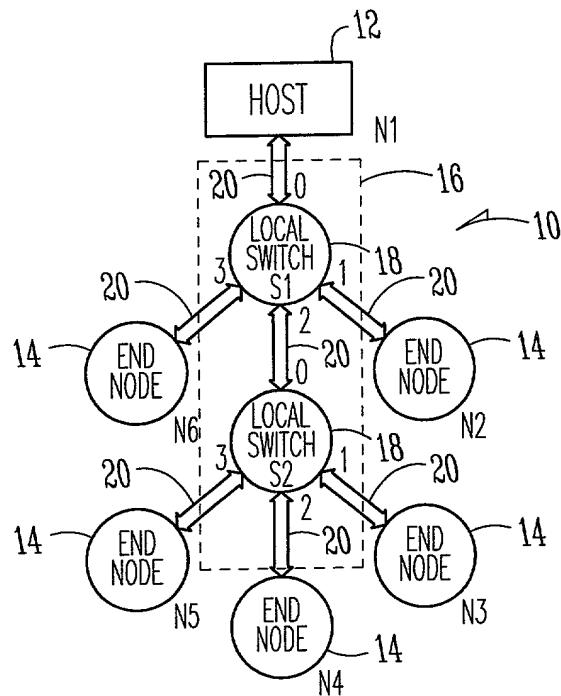


Fig. 1

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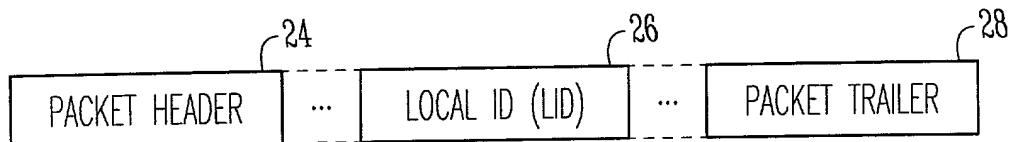


Fig. 2

S1 LOCAL		30	S2 LOCAL		32
NODE	PORT		NODE	PORT	
N1	0		N1	0	
N2	1		N2	0	
N3	2		N3	1	
N4	2		N4	2	
N5	2		N5	3	
N6	3		N6	0	

.. . *Fig. 3*

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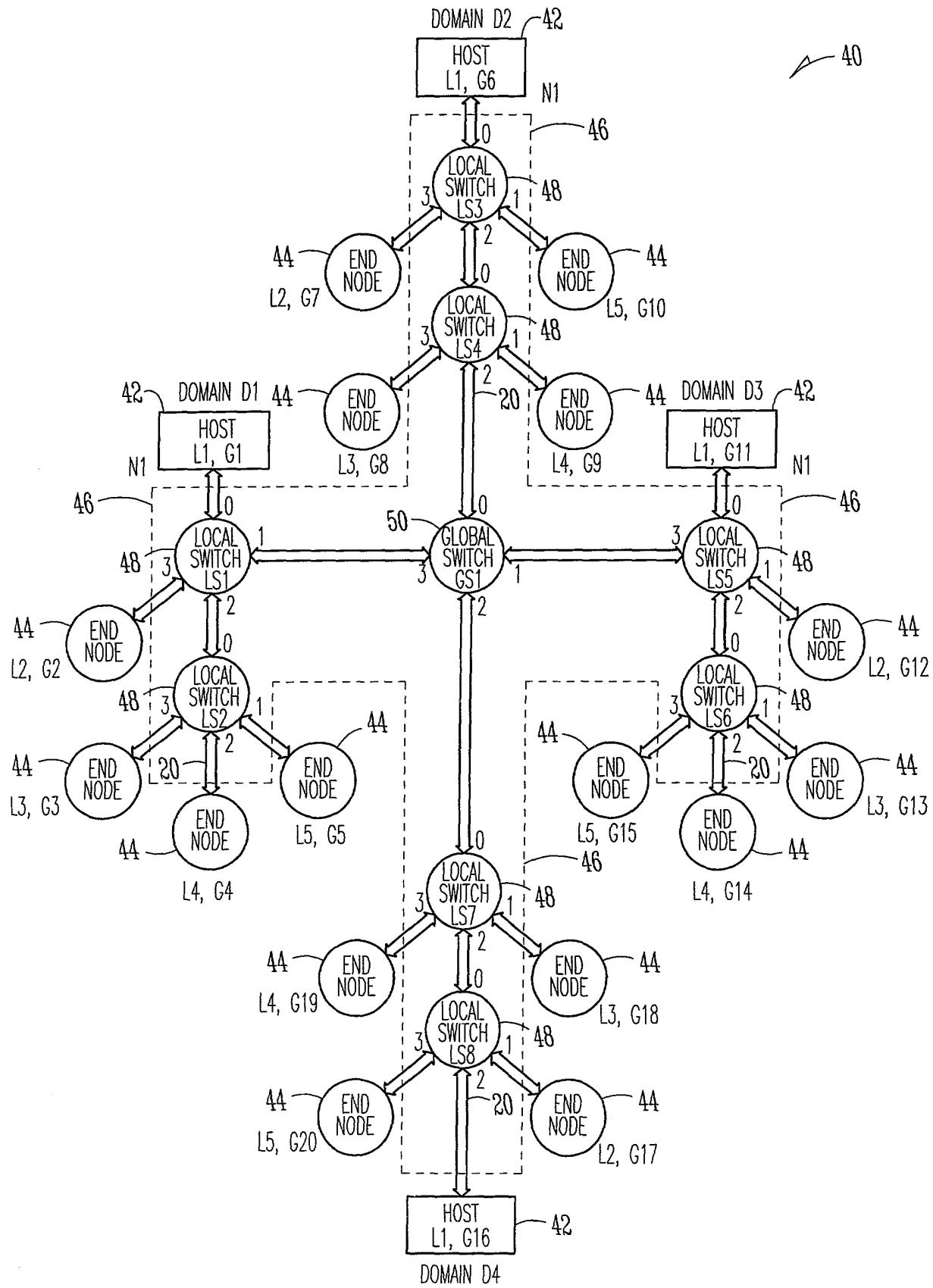


Fig. 4

TITLE: MULTIPLE-DOMAIN PROCESSING SYSTEM USING HIERARCHICALLY ORTHOGONAL
SWITCHING FABRIC
INVENTORS NAME: Oleg Awsienko et al.
SERIAL NO.: 10/005,895

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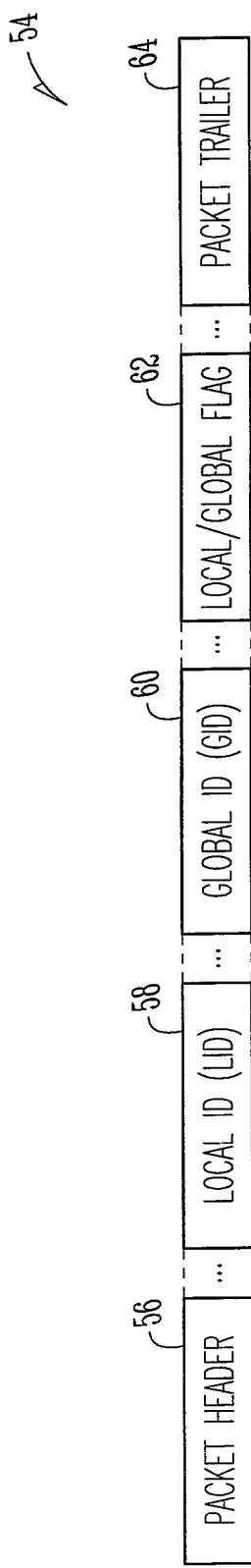
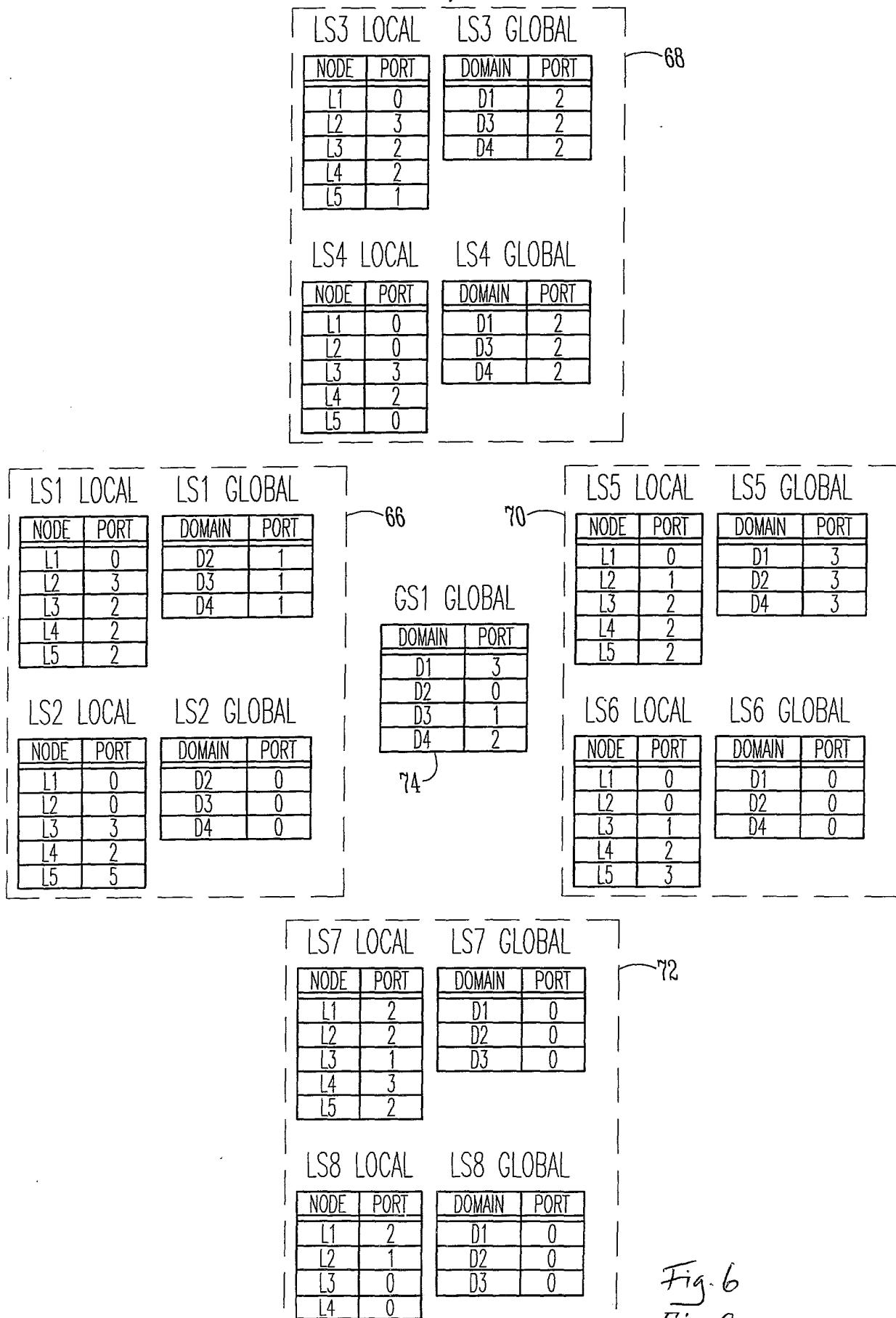


Fig. 5

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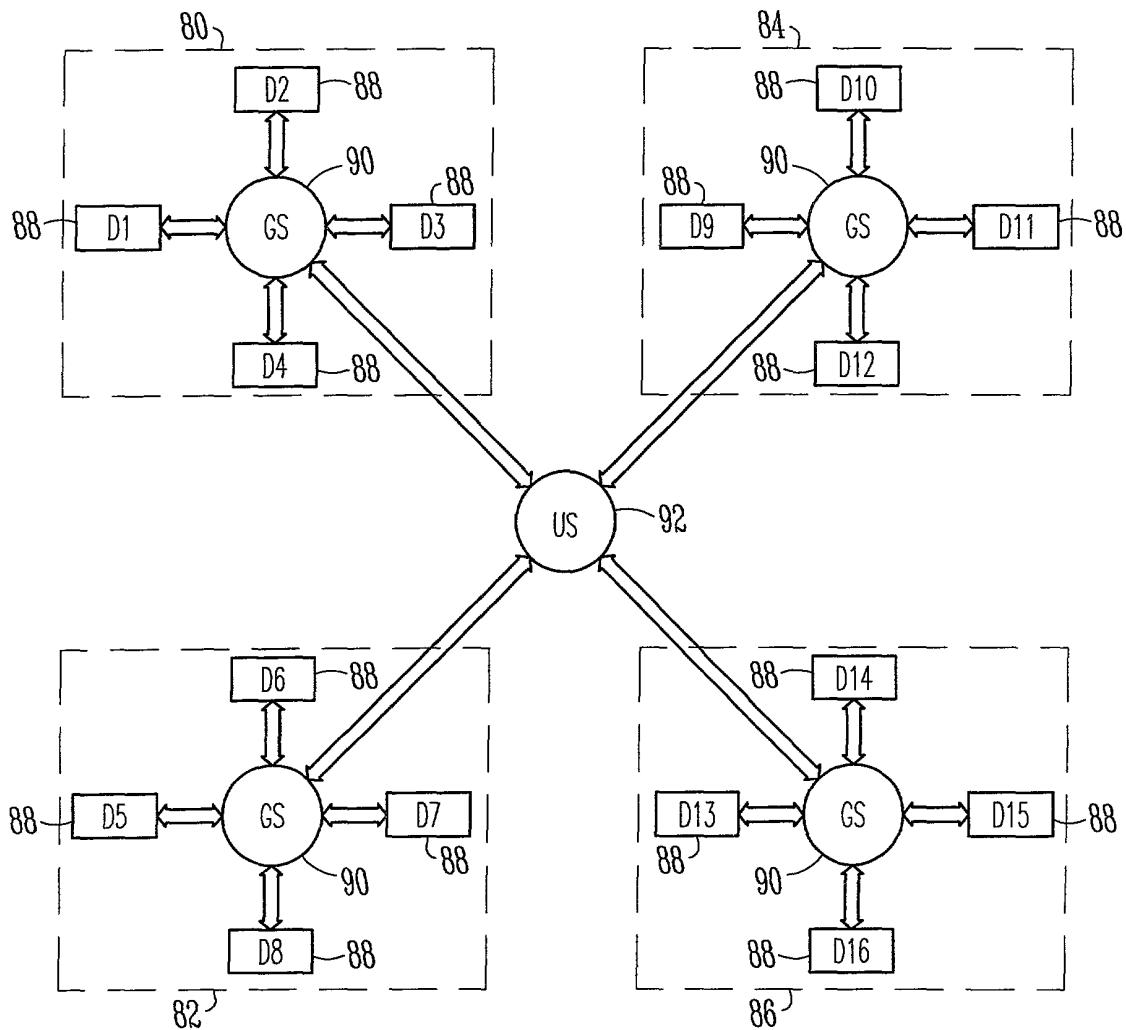


Fig. 7